(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 June 2005 (23.06.2005)

PCT

(10) International Publication Number
WO 2005/057718 A1

(51) International Patent Classification[7]: H01P 1/18, H03H 7/30

(21) International Application Number: PCT/SE2003/001918

(22) International Filing Date: 10 December 2003 (10.12.2003)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

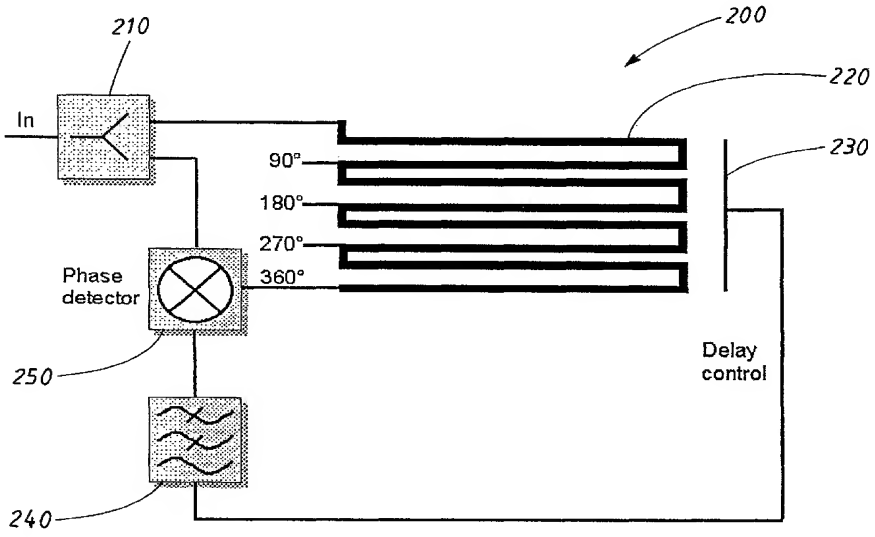
(84) Designated States *(regional)*: ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv)) for US only*

Published:
— *with international search report*

[Continued on next page]

(54) Title: A DELAY-LOCKED LOOP WITH PRECISION CONTROLLED DELAY



(57) Abstract: The invention discloses a delay-locked loop circuit (200) with input means (210) for a signal that is to be delayed, the input means comprising means for splitting the input signal into a first and a second branch. The signal in the first branch is connected to a component (220) for delaying the signal, and the signal in the second branch is used as a non-delayed reference for the delay caused by the delay component in the first branch. The delay component (220) is a passive tunable delay line, and the circuit comprises tuning means (230) for the tunable delay line, the tuning means being affected by said reference signal, and the first branch comprises output means for outputting a delayed signal with a chosen phase delay. Suitably, the delay component (220) is continuously tunable, for example a tunable ferroelectric delay line.

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